

Self-Assembled Molecular Nanowires for High Performance Organic Transistors

†Luke R. Fleet^{1,2}, †James Stott³, Byron Willis³, Salahud Din^{1,2}, Michele Serri^{1,2},

Gabriel Aeppli^{4-6,*}, Sandrine Heutz^{1,2,*} and Arokia Nathan^{3,7,*}

¹ Department of Materials, Imperial College London, London, SW7 2AZ, UK.

² London Centre for Nanotechnology, Imperial College London, London, SW7 2AZ, UK.

³ London Centre for Nanotechnology, University College London, London WC1H 0AH, UK.

⁴ Department of Physics, ETH Zürich, Zürich, CH-8093, Switzerland

⁵ Department of Physics, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, CH-1015, Switzerland

⁶ Photon Science Division, Paul Scherrer Institute, Villigen, CH-5232, Switzerland

⁷ Department of Engineering, Electrical Engineering Division, Cambridge University, Cambridge, UK.

†These authors contributed equally to this work

* Corresponding authors: Gabriel Aeppli: gabriel.aeppli@psi.ch; Sandrine Heutz: s.heutz@imperial.ac.uk; Arokia Nathan: an299@cam.ac.uk

Abstract

While organic semiconductors provide tantalising possibilities for low-cost, light-weight, flexible electronic devices, their current use in transistors — the fundamental building block — is rather limited as their speed and reliability is not competitive with their inorganic counterparts, and is simply too poor for many practical applications. Through self-assembly, highly ordered nanostructures can be prepared that have more competitive transport characteristics, but no simple, scalable method has been discovered that can produce devices based on such nanostructures. Here we show how transistors of self-assembled molecular nanowires can be fabricated using a scalable, gradient sublimation technique, which have dramatically improved characteristics compared to their thin film counterparts, both in terms of performance and stability. Nanowire devices based on copper phthalocyanine have been fabricated with threshold voltages as low as -2.1 V, high on/off ratios of 10^5 , small sub-threshold swings of 0.9 V/decade and mobilities of 0.6 cm²/Vs, and lower trap energies as deduced from temperature-dependent properties - in line with leading organic semiconductors involving more complex fabrication. High-performance transistors manufactured using our scalable deposition technique, compatible with flexible substrates, could enable integrated all-organic chips implementing conventional as well as neuromorphic computation and combining sensors, logic, data storage, drivers and displays.

Keywords:

Nanowire transistor, phthalocyanine, organic electronics, stability, mobility, temperature dependence, image analysis, neuromorphic computing.

Introduction

The ability to deposit organic semiconductors as thin films or nanostructures on a range of low cost, including flexible, substrates has led to applications ranging from gas sensors and smart tags to light emitting diodes and solar cells.¹⁻⁶ Despite those successes there are still many challenges, particularly given the need to integrate the organic devices with transistors, providing logic, data storage and drivers, which today are almost inevitably inorganic. Organic transistors have thus far not succeeded because they have yet to simultaneously achieve stability, reproducibility and scalability of manufacture.⁷ There has of course been great scientific progress on polymer-based electronics,⁸ but in principle, small aromatic molecules are more robust for processing and eventual use. Unfortunately, conventional polycrystalline thin film transistors, prepared using a variety of simple vacuum-based techniques such as organic molecular beam deposition (OMBD), typically exhibit mobilities on the order of $10^{-3} \text{ cm}^2/\text{Vs}$,^{7,9} much too low for many applications, with the transport limited by structural defects. The film mobility can be increased by improving the crystallinity⁵ but this often entails high temperature¹⁰ or patterned¹¹ growth, post-deposition annealing¹² or weak epitaxy.¹³ All of these methods greatly restrict the types of devices that can be created and also the scalability of manufacture. Organic nanowires, self-assembled into highly crystalline nanostructures, offer the tantalising prospect of overcoming the limitations stemming from grain boundaries, in simple experimental conditions (e.g. low vacuum deposition or self-assembly from solution, room temperature substrate).¹⁴

Earlier reports showing the potential of nanostructures focussed on the pentacene derivative hexathiapentacene (HTP), which lent itself to simple solution processing and drop-casting techniques for fabrication of large-area arrays of nanowire transistors.^{14, 15} P-channel devices based on HTP nanowires were demonstrated and later combined with *n*-channel perylenediimide nanowires leading to the first report of a low cost, scalable organic nanowire logic.¹⁶ Although these reports showed the manufacturing potential of self-assembled nanostructure transistors, the devices displayed poor operating characteristics, rendering them unsuitable for commercial applications. Subsequently, numerous articles discussed alternative techniques or systems but, despite promising advances in sensing,¹⁷ to our knowledge none have reported a simple, low cost, scalable solution capable of producing devices that can rival their inorganic counterparts.

Phthalocyanines (Pc's) are planar aromatic molecules which are attractive for self-assembled nanowire devices due to their stability, flexibility and tuneability.¹⁸ Their versatility arises from the fact that they are able to host many metal ions at their cores¹⁹ and can exist in a variety of crystal phases, controllable through growth conditions,^{18, 19} allowing their electronic structure to be modified. Copper phthalocyanine (CuPc) has been used in blue dyes and paints since the 1930s due to its chemical stability and optical properties,²⁰ and has already been shown to self-assemble into nanostructures with e.g. single-crystal nanoribbon devices exhibiting reasonable characteristics.²¹⁻²⁹ It has a long-standing tradition in photovoltaics, with a history spanning the first two-layer small molecule solar cell⁶ to recent fundamental studies in band structure engineering.³⁰ Phthalocyanines are also key components in new research directions such as organic spintronics where their

spin can be exploited to modulate transport^{31, 32} or store information.^{33, 34} Here we demonstrate that it is possible to create organic field effect transistors of CuPc nanowires that have characteristics approaching those of polycrystalline silicon devices. The random network architecture may enable exploitation for neuromorphic computing,^{35, 36} with the nanowires representing neurons and their intersections analogous to synapses, in addition to conventional logic. Furthermore, as this was performed using conventional gradient sublimation with no post-deposition processing or expensive selection (as required for example for carbon nanotube-based electronics), the fabrication process is simple, low cost and scalable.

Results and discussion

Deposition of organic nanowires

The face-to-face (π -stack) stacking in planar aromatic molecules, arising from the strong π - π interactions³⁷ leads to a large overlap of the electronic wave functions in adjacent molecules. This causes an increase in the bandwidths which directly correlate with electrical conductivity in the coherent transport regime, thus resulting in high mobilities.^{38, 39} Due to its simplicity, organic vapour phase deposition (OVPD) is a popular technique for creating self-assembled nanostructures.^{17, 40} Although OVPD has been successful in generating a wide range of nanostructures of different molecules,¹⁴ high mobility transistors using conventional substrates without the need for post- or pre-deposition processing have so far remained elusive.^{14, 41}

CuPc nanostructures, grown by physical vapour transport, were first reported in 2006 yielding structures in the form of β -phase nano-ribbons approximately hundreds of nanometres wide and 5-10 μm in length.^{21, 22} The transport properties of individual ribbons were explored using micromanipulation and found to exhibit hole mobilities of the order of $0.1 \text{ cm}^2/\text{Vs}$.²³ There have been many developments since,^{17, 26, 27} such as air dielectrics²⁴ and combinations with fluorinated CuPc to demonstrate logic gates,²⁵ but this technique, although of great interest for the study of fundamental transport properties, is not practical for large scale application. In 2010 a new type of CuPc nanostructure was reported: η -phase nanowires.²⁸ These nanowires are approximately 10-100 nm in width and up to a centimetre in length. These directional, high aspect ratio nanowires are ideal for use in organic transistors, due to the low density of structural defects, and it is the transport characteristics of devices prepared using these nanowires that are reported here.

Figure 1 shows the simple setup of a conventional OVPD system to create self-assembled nanostructures. A different tube furnace was used to that of the previous report,²⁸ one with a radius more than twice larger, showing that this technique is, to some degree at least, scalable. An inert carrier gas, nitrogen in our case, is used to transport sublimed molecules from the hot end of a split tube furnace to the cool end, approximately 1 m away. Substrates were positioned at the cool end of the chamber in a region held at approximately room temperature, meaning that a large range of substrates can be used. The substrates were mounted at a height approximately half of the tube diameter, 2 cm, although the exact position is not important as nanowires form across the whole tube within a region of approximately 30 cm outside the furnace. Structural characterisation confirmed that the nanowires were in the η -phase, with the π -stacking occurring along the long wire axis. Our previous work on the magnetic properties of the nanowires show that the Cu^{2+} ions are coupled *via* a small exchange interaction, successfully modelled by density functional theory²⁸, which results in a Curie-Weiss-dominated magnetic response down to low temperatures. Coupled with our optical absorption analysis, this result confirms the integrity of the material and the absence of impurities, e.g. copper oxides. Although the nanowires had some directionality, preferentially growing between the electrodes due to the carrier gas flow, the devices are most appropriately described as consisting of a nanowire network. Many nanowires did not span fully between the electrodes and many were intertwined. The effect of the nanowire network on the transport properties will be discussed in detail later.

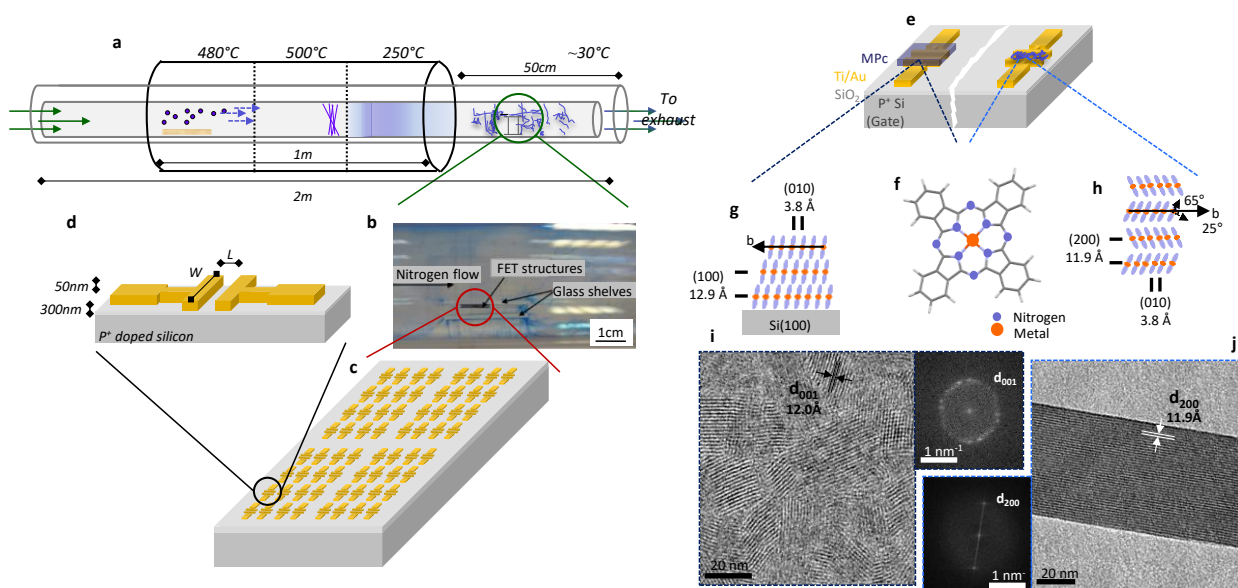


Figure 1 | Manufacturing nanowire transistors. **a**, Organic vapour phase deposition of CuPc nanowires using gradient sublimation in a conventional 3-zone furnace. **b**, photograph of CuPc nanowires growing on and around a substrate. **c**, 48 devices were prepared onto a doped silicon wafer: 8 of each length for 6 channel lengths (5-50 μm), all with a width of 500 μm . **d**, The devices were back-gated 3-terminal transistor substrates made with doped silicon, 300 nm silicon dioxide with 50 nm gold contact. A 1 nm titanium layer was used to help the electrodes adhere to the oxide. **e**, Nanowires were deposited directly onto the substrates using OVPD, with 50 nm CuPc thin film transistors also prepared, for comparison, using organic molecular beam deposition. **f**, Planar metal phthalocyanine molecule. **g**, Stacking of α -phase CuPc on silicon showing the stacking axis lie approximately parallel to the substrate. **h**, Stacking arrangement of CuPc nanowires in the η -phase. **i**, TEM images of CuPc thin films along with Fourier transform showing a 12.1 \AA spacing corresponding to the (001) plane of α -phase CuPc. **j**, TEM images of CuPc nanowire along with Fourier transform showing a 12.0 \AA spacing corresponding to the (200) plane of η -phase CuPc. This shows that the stacking axis lies along the long axis of the nanowires.

For comparison of the transport characteristics, 50 nm thick CuPc thin film devices were also prepared using conventional OMBD onto the same substrates (supplementary information). The polycrystalline films were deposited at room temperature, forming in the α -phase,⁴² with a median crystallite size of ~ 40 nm, determined using X-ray diffraction. The stacking axis was determined to be parallel to the substrate so, as in the case of the nanowire devices, the current preferentially flows in the plane parallel to the substrate. TEM images of the nanowires and thin films can be seen in figure 1.i, j, clearly showing the reduced number of structural defects of the nanowires. Analysis of the TEM lattice fringes confirms the molecular orientation, with the (001) spacing (12.0 Å) visible in the thin films and (200) spacing (11.9 Å) present for the nanowires.

Performance of CuPc nanowire transistors

We begin by emphasising that all devices were deposited at room temperature and had no post-deposition treatment. Some important parameters to consider when analysing the transport in thin film transistors are the mobility, threshold voltage, subthreshold swing and on/off ratio. In the standard Shockley FET model the linear I_d^{lin} and saturation I_d^{sat} currents are given by:

$$I_d^{lin} = \mu C_{ox} \frac{W}{L} \left(V_g - V_t - \frac{V_d}{2} \right) V_d \quad (1)$$

$$I_d^{sat}(V_g) = \mu C_{ox} \frac{W}{2L} (V_g - V_t)^2 \quad (2)$$

where I_d is the drain current, μ the mobility, V_d the drain bias, V_g the gate bias, V_t the threshold voltage, L the channel length, W the channel width and C_{ox} the oxide capacitance per unit area. The subthreshold swing is defined as:

$$S = \frac{dV_g}{d(\log I_d)} \quad (3)$$

and gives an effective measure of the steepness of device turn-on.

Figure 2 shows the typical transfer and output curves for CuPc nanowire and thin film transistors with a channel length of 50 μm . Depending on the CuPc polymorph, the devices exhibit very different input-output characteristics. There are several advantages for the nanowire devices. Apart from the low operating voltages, the most striking is the steep turn-on or small subthreshold swing.

Table 1 | Comparison of CuPc thin film and nanowire transistors.

	CuPc thin film transistor		CuPc nanowire transistor	
	Median	MAD	Median	MAD
Threshold voltage, V_t (V)	-10	2.7	-2.1	0.5
Mobility, μ ($\times 10^{-3}$ cm ² /Vs)	0.4	0.1	3.6*	0.4
Hysteresis	4.8	0.9	0.2	0.1
On/off ratio	10 ⁴	-	10 ⁵	-
Subthreshold slope, S (V/decade)	4.3	0.8	0.9	0.4

Threshold voltage, mobility, hysteresis, on/off ratio and subthreshold slope for CuPc thin film devices with a source-drain bias of -40V and CuPc nanowire devices with a source-drain bias of -10V. MAD = median absolute deviation. * This value needs correcting by a factor of ~150, as discussed in the text.

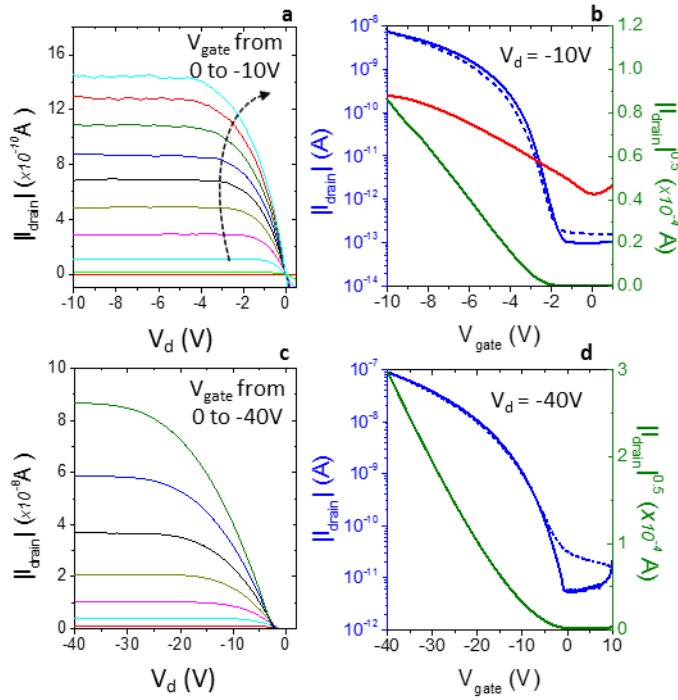


Figure 2 | Device characteristics at room temperature. **a,b**, Typical output and transfer curves for CuPc nanowire transistors with a channel length of 50 μ m. **c,d**, Typical transfer and output curves for 50nm CuPc thin film transistors grown onto the same substrates. The red line in figure **b** shows the transfer curves measured for CuPc nanoribbons.²¹

Although the characteristics shown are for one transistor, the devices were found to be highly reproducible (supplementary information). The average device characteristics from all 48 nanowire devices are shown in table 1, along with the parameters extracted from CuPc thin film devices. The characteristics for both sets were determined in the saturation regime, at a source-drain bias -10 V for the nanowire and -40 V for the thin film devices. It should also be noted that the nanowire device had a very weak dependence on the channel length (supplementary information). This most likely arises due to the fact that in longer channel length devices the nanowire network changes greatly, with a larger number of wires no longer spanning the full length of the

contact. The contact resistance was not observed to be significant in these devices, with no sub-linear rise of the drain current observed.

Table 1 reveals that the nanowire devices have much lower threshold voltage, hysteresis and subthreshold swings. The devices exhibit fairly similar mobilities but this value of the mobility constitutes a lower limit since the channel width for the devices is much less than 500 μm due to incomplete coverage of the nanowires over the whole channel. This will be discussed in more detail in later sections but it is worth pointing out that even without this correction the nanowire devices are attractive candidates for applications due to their ease of deposition, low voltage operation and low subthreshold swing – comparable to single crystal pentacene.⁴³

One of the problems with conventional organic transistors is the non-linearity of the transfer curves which arises due to the large trap densities. This type of curving is clearly seen in the nanocrystalline CuPc thin film characteristics, and is somewhat expected due to the large number of grain boundaries. These non-linearities can make it difficult to extract values for the mobility and threshold voltage as the conventional FET models rely on a linear relationship of the transfer curves in the linear regime and a quadratic dependence in the saturation regime. The linear behaviour is clearly seen in the nanowire characteristics making these devices of particular interest for understanding the fundamental transport mechanisms.

Stability of CuPc nanowire devices

CuPc has been used as a dye since the 1930's not just due to its optical properties but also for its stability, which also makes it an attractive molecule for electronics. As oxidising agents are known to have a significant effect on the transport properties of CuPc⁴⁴ the effects of ageing have been explored in both the CuPc nanowire and thin film devices. A selection of devices was left in air, in the dark, for 6 months and the transistor characteristics re-measured. It can be seen from figure 3 that in the thin films, ageing caused a dramatic shift in the threshold voltage from $-10(\pm 3)$ V to $+30(\pm 12)$ V. The threshold voltage shift is most likely due to additional internal potential drops derived from the absorption of oxidising gases, an effect greatly influenced by crystallinity and morphology as the concentration of absorption sites is related to structural defects including surfaces such as grain boundaries. In particular, nanowire devices could have much greater stability due to the reduced number of grain boundaries. This was found to be the case, with a much smaller shift of the average threshold voltage from $-5.5(\pm 0.9)$ V to $-3.8(\pm 1.6)$ V observed. The mobility in all devices was found to have increased slightly by $\sim 0.14 \times 10^{-3} \text{ cm}^2/\text{Vs}$ after 6 months. The exceptional stability of the nanowires makes them candidates for commercial applications.

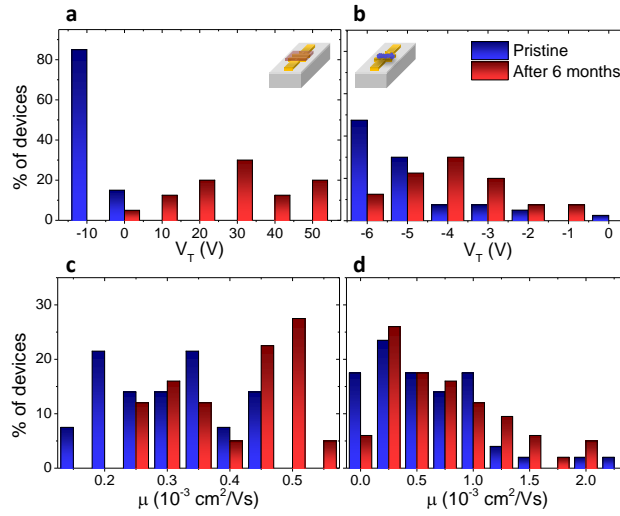


Figure 3] Stability of copper phthalocyanine. Effect of ageing on the **a,b**, threshold voltage and **c,d**, mobility of CuPc **a,c**, thin film and **b,d**, nanowire transistors.

Temperature-dependent transport

To explore further the hole transport in the transistors, we measured the temperature dependence of the device performance. The devices were cooled using a Quantum Design Physical Properties Measurement System (PPMS), and kept in the dark under a vacuum of $\sim 10^{-4}$ mbar. Figure 4 shows the transfer curves for the thin film and nanowire devices, with the source-drain bias held at -10 V, for a range of temperatures. It can be seen from figure 4 that the nanowire devices have better device characteristics with much weaker temperature dependence, much lower threshold voltages, much faster turn-on's (low subthreshold swing) and much higher

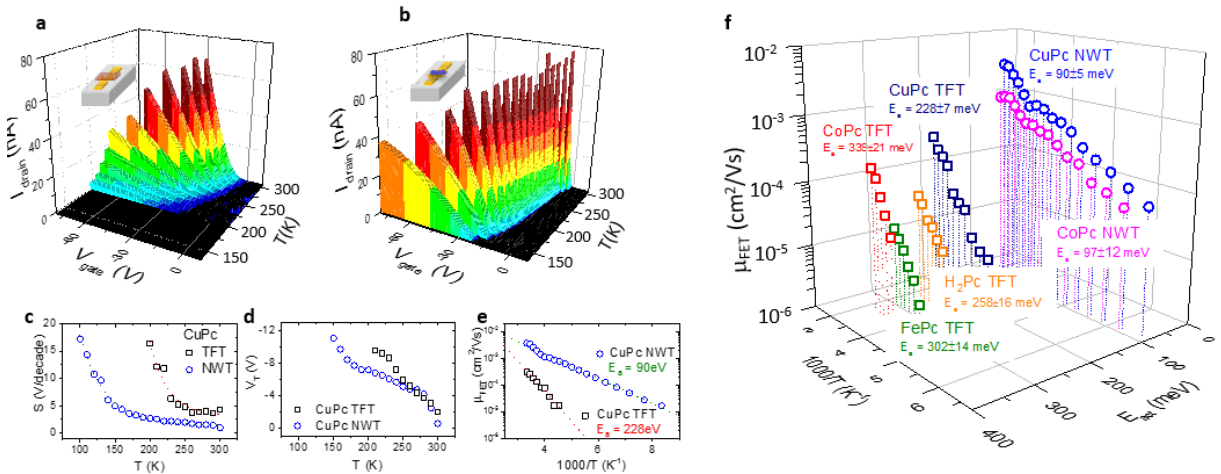


Figure 4] Temperature dependence of the devices. Transfer curves for CuPc **a**, thin film and **b**, nanowire transistors taken at a range of temperatures for $V_d = 10$ V. The extracted device parameters; **c**, subthreshold swing, **d**, threshold voltage, **e**, mobility; are shown as a function of temperature. From **e**, the Arrhenius plot of the mobility, activation energy was extracted. **f**, A comparison of the activation energies of the mobility for (Cu, Fe, Co, H₂)Pc thin films as well as (Cu, Co)Pc nanowire transistors.

currents at low temperature. The weaker temperature dependence appears not just in the currents but also in the other parameters: as the devices are cooled the threshold voltage increases, the subthreshold slope increases and the current decreases much faster for the thin film counterparts. The thermally activated behaviour observed is typical of conventional organic devices in which the transport is dominated by traps. This becomes more apparent when the mobility is plotted against $1/T$, following the conventional Arrhenius behaviour, see figure 4.f. The activation energy is only weakly dependent on the gate bias (supplementary information) for both sets of devices, suggesting that the transport is dominated by a discrete trap energy⁴⁵. As expected from the increased disorder, the activation energy for the thin films ~ 0.23 eV is much larger than that for the nanowires ~ 0.09 eV. As the nanowires are highly crystalline one may expect to see a weak temperature dependence at high temperature – signatures of band-like transport, which has been previously observed and modelled for highly crystalline molecular semiconductors.⁴⁶⁻⁴⁸ This was not observed in these devices as the transport occurs across a nanowire network in which hopping between the nanowires is strongly temperature-dependent. The activation energies shown in figure 4 were extracted for temperatures below 250K where this effect is less significant (see supplementary information).

One property that makes metal Pc's particularly interesting and useful as organic semiconductors is that these molecules host different types of central metal ions, allowing control of electronic, optical and magnetic properties *via* the filling of their outer (generally d) orbitals. This has been studied theoretically and there are a few experimental reports discussing such control in the context of magnetic properties.⁴⁹⁻⁵¹ Determining the effect of the d-orbitals in thin film transistors with a large number of structural defects is, however, extremely challenging.^{52, 53} To highlight this, Co, Fe and metal-free H₂Pc devices were prepared using the same deposition parameters as the CuPc thin films. The transistor characteristics were found to be much more non-linear with the activation energies varying between 0.23 – 0.34 eV and the mobilities by up to an order of magnitude (supplementary information). The increased variability suggests that the d-orbitals may have a strong influence on the transport in phthalocyanines, but to access the intrinsic materials properties a more ideal system with reduced defects would be needed. To address this, we measured the transport properties of CoPc nanowire transistors, prepared using the same vapour deposition conditions and found to have the same structure as CuPc (see supplementary information). Thus, the preparation of self-assembled nanostructures presented here is not unique to CuPc but can also be applied to other MPC's. The CoPc nanowire devices exhibited almost identical characteristic to the CuPc nanowire devices, shown in figure 4f. Contrary to what was observed in the MPC thin film devices and perhaps expected based on knowledge of the transition metal-dependent magnetism, the gated charge transport is not strongly dependent on the transition metal at the centre of the phthalocyanine molecules. We therefore suspect that the changes in the thin film characteristics were most likely arising from the lower purity of the other phthalocyanines, with the self-assembled growth of the nanowires helping to reduce the number of impurities, in analogy with the purification which occurs upon whisker growth and zone refinement in metallurgy, and also because post-growth diffusion of contaminants is reduced in the absence of grain boundaries.

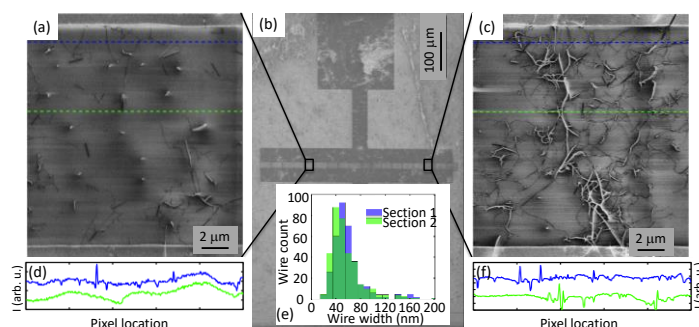


Figure 5 | Image analysis of nanowire coverage. Wire width estimates: **a**, and **c**, high resolution scanning electron micrograph of low and high wire density regions respectively, **b**, low resolution scanning electron micrograph of complete NW device, **d**, and **f**, instantaneous pixel intensity cross-sections at marked locations on **a**, and **c**, and **e**, summary of all wire widths from complete device.

Nanowire image analysis

We have mentioned previously that the extracted values of the mobility for nanowire devices actually represent lower limits because the nanowires do not cover the entire channel width. As the conductance scales with channel width, the nanowire network geometry will have a dramatic effect on the apparent mobility. We explored the nanowire coverage using scanning electron microscopy, with typical images of a device shown in figure 5. It can be seen that there exist regions with a large density of nanowires as well as regions which are very sparsely covered. Apart from direct conduction paths, with one wire spanning the full channel length, there are also indirect conduction paths, which affect the channel width. Furthermore, the nanowires do not take a direct path between the electrodes, which means that the channel length also needs correcting. Several methods were employed to determine the coverage of nanowires: full wire detection, counting pixel-by-pixel; regional sampling and extrapolation; and line-by-line counting and extrapolation (full details of the image analysis can be found in the supplementary information).

The last factor that needs to be taken into account is the capacitance of the devices. When extracting a value for the mobility, the capacitance per unit area was assumed to be associated with a uniform dielectric of constant thickness. This assumption is incorrect because a significant fraction of the semiconducting material which connects the source and drain contact is not in direct contact with the dielectric surface and therefore also separated from it by either an air or vacuum gap, depending on the measurement environment. Details for correcting the capacitance can be found in the supplementary information.

The resulting correction factors are estimated to increase the likely mobility as follows: channel width $\times 2.7$; capacitance $\times 2$; continuous paths $\times 2$; indirect paths $\times \sqrt{2}$. The cumulative correction is therefore $\times 15.3$. Applying this correction to the mobility of the nanowire devices suggests that the mobilities are actually in the region of $0.6 \text{ cm}^2/\text{Vs}$. This value is larger than that reported for both CuPc nanoribbons²³ and similar to that reported in CuPc single crystals.²⁹ What is particularly noteworthy about this mobility value is that the gated medium in our devices is a nanowire network, with charge hopping between wires. Therefore the mobility in the individual nanowires is significantly higher than $0.6 \text{ cm}^2/\text{Vs}$, a value itself competitive with other organic semiconductors,

as will be discussed, but particularly impressive considering the ease of fabrication and the simple device architecture.

Performance of organic transistors

The advantage of CuPc nanowire transistors over conventional organic devices is their ease of deposition, low operating voltage and high stability. When taking into account the correction factors above, the extracted mobility is competitive with many other organic devices, particularly considering that these devices were prepared on conventional substrates with a silicon dioxide interface, known to lead to a large interface trap density. To underscore the performance of the nanowire devices, the threshold voltage, subthreshold slope and mobility of some of the leading organic semiconductors used in transistors are compared in figure 6, all with SiO₂ as the dielectric interface.^{15, 43, 54-62} It can be seen that the low threshold voltage and subthreshold swing of the nanowire transistors puts them on the same level as polycrystalline pentacene^{54, 58} and single crystal TIPS-pentacene⁵⁹ and rubrene^{54, 56} devices. The mobility is similar to that of polycrystalline pentacene, which is one of the most popular systems for organic thin film transistors, and not far behind that of single crystal pentacene and rubrene. As the mobility of individual wires is expected to be significantly higher than that obtained for the network devices the mobility could exceed that of the leading organic semiconductors.

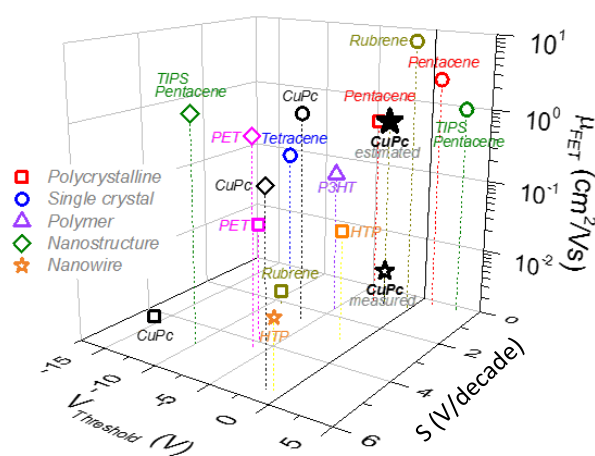


Figure 6] Performance of CuPc nanowire devices. Comparison of the mobility, threshold voltage and subthreshold swing for some of the most studied, and currently most promising, organic materials used in field-effect transistors.

As was already mentioned the mobility of the nanowire devices is similar to that of single crystal CuPc but the devices exhibit much lower threshold voltages. It is also worth pointing out that these devices perform much better than the previously reported CuPc nanoribbons, particularly when it comes to the subthreshold slope²³. To the best of our knowledge, there is currently only one other report of (network-based) nanowire transistors that have been employed in a similar way to that reported in this paper. These devices based on HTP, however,

exhibit very high subthreshold slopes and low mobilities. A more detailed comparison of the performance of different organic thin film transistors can be found in the supplementary information.

Conclusions

Employing the simple method of gradient sublimation we have shown that it is possible to create self-assembled nanowire transistors with low threshold voltage, subthreshold slope and good mobility. We show a method for analysing nanowire devices, which provides to a reasonable degree correction factors for the channel width and length, applicable to other network transistors. After correcting for effective dimensions and the capacitance, the mobility is estimated to be $0.6 \text{ cm}^2/\text{Vs}$ on conventional Si/SiO₂ substrates, a value comparable to single crystal CuPc devices and polycrystalline pentacene. The mobility for individual nanowires is likely to be much higher than this and could exceed that of leading organic single crystals. After storage for 6 months, the nanowire devices show little degradation, demonstrating their practical suitability. Exploring the temperature dependence of CuPc along with other Pc's, we showed that the transport is dominated by structurally-induced traps. Temperature dependent transport measurements show that the effective trap depth is significantly reduced in nanowire devices, compared to thin films, making them interesting for the study of fundamental transport mechanisms. Employing the same growth conditions, we show that it is possible to deposit other MPc's, and transport analysis of CoPc devices suggests that the *d*-orbitals have a much weaker effect than suggested by thin film devices. Finally, the similarities of the random network formed by the nanowires between source and drain to that of neural circuits suggests further studies to consider applications for neuromorphic computing.^{35, 36}

Methods

Substrate fabrication

Doped crystalline silicon wafers were cleaned in a sulphuric acid (H₂SO₄)-hydrogen peroxide (H₂O₂) solution and hydrofluoric (HF) acid to remove any surface oxide, before being rinsed in DI water and blown dry with dry nitrogen gas. A 300nm SiO₂ layer was deposited at 300°C using plasma enhanced chemical vapour deposition using a multi-chamber parallel plate system from MVSsystems, with 13.56 MHz radio frequency source. 1nm titanium, followed by 50nm of gold, was then deposited using a thermal evaporator and conventional photolithography techniques.

OMBD Sample growth

MPC films were deposited using conventional organic molecular beam deposition (OMBD), using a commercial Kurt J. Lesker SPECTROS system. Commercial powders, purchased from Sigma-Aldrich, were purified twice using conventional gradient sublimation in a vacuum of $\sim 10^{-2}$ mbar and nitrogen carrier gas. 50 nm films, deposited at 0.5 Å/s, were grown onto silicon, glass and bottom-gate, bottom-contact transistors. The depositions were performed using an effusion cell, with a chamber base pressure of 3×10^{-7} mbar, at room temperature. The substrates were rotated during the deposition to ensure uniform film growth. The samples were then stored in nitrogen.

OVPD Sample growth

The OVPD system consists of a quartz tubular chamber (2 m long and 4 cm in diameter) inserted into a three-zone Elite furnace where the temperature of the individual zones (each ~ 33 cm in length) can be independently controlled. The flow of the nitrogen carrier gas is controlled by a variable area flowmeter giving a rate of 1 litre/minute. The base pressure of the chamber is $\sim 10^{-2}$ mbar before introducing nitrogen gas and increases to 10 mbar during the growth. The (Cu,Co)Pc powder (Aldrich) was twice purified using gradient sublimation. The temperature of the furnace at the first, second, and third zone during deposition is 480, 320, and 250 °C, respectively. Growth times are reported from the moment the heating is started from room temperature conditions, so that the final source temperature is attained after a growth time of 60 min.

Conventional 3-terminal bottom-gate, bottom-contact transistor structures were placed in the region of the nanowires, left for up to 72 hours to allow time for the nanowires to cover a large portion of the substrate area. Each substrate consisted of 48 devices: 8 devices for 6 channel lengths ranging from 5 to 50 μm , all with a channel width of 500 μm . The devices had a 300 nm silicon dioxide layer, prepared on a p^+ doped silicon substrate, with 50 nm gold contacts deposited using conventional photolithography techniques and thermal evaporation. A thin 1 nm titanium layer was used to help the electrodes adhere to the oxide surface.

Electron Microscopy

The morphology of the samples on silicon was investigated with a LEO 1525 Gemini FEGSEM (5kV), on samples coated with a thin (10-15 nm) chromium layer. High resolution images of MPC's, deposited directly onto Cu grids, were obtained with a JEOL 2010 TEM (200 kV).

Electrical characterisation of devices

Current-voltage (IV) measurements were carried out using a Keithley 4200 semiconductor characterisation system (SCS) with 4 source-measure units (SMUs), each coupled to a pre-amplifier allowing sub-fA current

resolution. To reduce noise, room temperature measurements were performed in conjunction with a Signatone shielded probe station using triax cabling. To measure the transistors at lower temperatures the devices were cooled using a quantum design PPMS system at a rate of approximately 20 K/hour.

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Author contributions

J. Stott prepared the transistor substrates, characterised the CuPc nanowire and thin film devices at room temperature and performed the image analysis. S. Din prepared CuPc nanowire and thin film devices and assisted in the room temperature characterisation. L. Fleet prepared and characterised thin film devices of (Cu, Co, Fe, H₂)Pc and nanowire devices of (Cu,Co)Pc with assistance of M. Serri, with the temperature dependent measurements carried out with B. Villis. S. Heutz, G. Aepli and A. Nathan provided technical input on materials and TFT analyses. The paper was written by J. Stott and L. Fleet, with all the authors discussing the results and the preparation of the manuscript.

Supporting information

Device reproducibility (Figures S1-S2); Contact resistance (Figure S3); Comparison of CuPc thin film and nanowire transistor characteristics (Table S1); Transport in MPc thin films (Figure S4); Comparison of phthalocyanine thin film transistors (Table S2). Correcting the mobility: Image analysis approaches (Figure S5); Nanowire detection (Figure S6); Nanowire connectivity (Figure S7); Summary of corrections (Table S3). Nanowire temperature dependence (Figure S8); Comparison with other organic semiconductors (Figure S9); Switching characteristics (Figure S10).

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